

64Mx72, 128Mx72, 256Mx72, DDR2 ECC DIMM Module

Registered ECC DDR2 DIMM, based on 64Mx4 or 128Mx4, 4 bank, 1.8V, DDR2 SDRAMs

General Description

These Legacy devices are JEDEC standard registered ECC DIMM modules, based on CMOS DDR2 SDRAM technology, and are available in 64Mx72 (512MB), 128Mx72 (1GB), and 256Mx72 (2GB). These devices consist of 18 or 36 CMOS DDR2 SDRAMs in FBGA packages on a 240-pin glass epoxy substrate.

The memory array is designed with Double Data Rate (DDR2) Synchronous DRAMs for ECC applications. All control and address signals are regenerated on the DIMM using register devices and a PLL for clock distribution. This reduces capacitive loading on the memory bus, but adds one clock cycle to SDRAM timings. Decoupling capacitors are mounted on the PCB board and Canopy™ in parallel for each DDR2 SDRAM, which provides proper voltage supply impedance over the entire frequency range of operations, in accordance with JEDEC specifications.

The Canopy™ leadless FBGA component carrier is part of Legacy Electronic's patented, three-dimensional assembly technology and is an alternative to conventional chip stacking.

These modules feature Serial Presence Detect (SPD) based on a serial EEPROM device, using the 2-pin I²C protocol. The first 128 bytes are programmed with configuration data and the second 128 bytes are available to the customer.

Features

- 240-pin Registered 8-Byte ECC DDR2 SDRAM Memory Module for PC, Workstation and Server main memory applications
- Impedance controlled multilayer leadless Canopy™ Technology
- Dual rank organization (128Mx72 and 256Mx72)
- JEDEC standard 1.8V I/O (SSTL_18-compatible)
- V_{DD} = +1.8V ± 0.1V, V_{DDQ} = +1.8V ± 0.1V
- 4-bit prefetch architecture
- Differential data strobe (DQS, DQS#) option
- Differential clock inputs (CK, CK#)
- Programmable CAS Latencies (3, 4, and 5), Burst Length (4 and 8)
- Posted CAS# additive latency (AL): 0, 1, 2, 3 and 4
- Auto Refresh (CBR) and Self Refresh Mode
- Phase-lock loop (PLL) clock driver to reduce CLK loading
- Off-Chip Driver (OCD) Impedance Adjustment
- On-Die Termination (ODT) supports termination values of 50, 75, and 150 ohms
- Serial Presence Detect (SPD) with EEPROM
- Module layout is based on JEDEC standard routing guidelines
- Impedance controlled 10-layer PCB Technology
- DQS edge-aligned with data for READs
- DQS center-aligned with data for WRITEs
- DLL to align DQ and DQS transitions with CK
- JEDEC standard form factor (133.35 mm x 21.6 mm)

Ordering Information:

x = DRAM Supplier	yy = Timing
L = Legacy	5.0 = PC2-3200 CL3.3.3
M = Micron	3.7 = PC2-4200 CL4.4.4
S = Infineon	3.0 = PC2-5300 CL4.4.4

Address Table

	512MB	1GB	1GB	2GB
Refresh Count	8K	8K	8K	8K
Row Addressing	8K (A0 ~ A12)	8K (A0 ~ A12)	16K (A0 ~ A13)	16K (A0 ~ A13)
Device Bank Addressing	4 (BA0, BA1)	4 (BA0, BA1)	4 (BA0, BA1)	4 (BA0, BA1)
Device Configuration	256Mb (64Mx4)	256Mb (64Mx4)	512Mb (128Mx4)	512Mb (128Mx4)
Column Addressing	2K (A0 ~ A9, A11)	2K (A0 ~ A9, A11)	2K (A0 ~ A9, A11)	2K (A0 ~ A9, A11)
Module Rank Addressing	1 (S0#)	2 (S0#, S1#)	1 (S0#)	2 (S0#, S1#)

Pin Configurations (Front Side, Back Side)

PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL
1	V _{REF}	31	DQ19	61	A4	91	V _{SS}
2	V _{SS}	32	V _{SS}	62	V _{DDQ}	92	DQS5#
3	DQ0	33	DQ24	63	A2	93	DQS5
4	DQ1	34	DQ25	64	V _{DD}	94	V _{SS}
5	V _{SS}	35	V _{SS}	65	V _{SS}	95	DQ42
6	DQS0#	36	DQS3#	66	V _{SS}	96	DQ43
7	DQS0	37	DQS3	67	V _{DD}	97	V _{SS}
8	V _{SS}	38	V _{SS}	68	NC	98	DQ48
9	DQ2	39	DQ26	69	V _{DD}	99	DQ49
10	DQ3	40	DQ27	70	A10/AP	100	V _{SS}
11	V _{SS}	41	V _{SS}	71	BA0	101	SA2
12	DQ8	42	CB0	72	V _{DDQ}	102	NC
13	DQ9	43	CB1	73	WE#	103	V _{SS}
14	V _{SS}	44	V _{SS}	74	CAS#	104	DQS6#
15	DQS1#	45	DQS8#	75	V _{DDQ}	105	DQS6
16	DQS1	46	DQS8	76	S1#	106	V _{SS}
17	V _{SS}	47	V _{SS}	77	ODT1	107	DQ50
18	RESET#	48	CB2	78	V _{DDQ}	108	DQ51
19	NC	49	CB3	79	V _{SS}	109	V _{SS}
20	V _{SS}	50	V _{SS}	80	DQ32	110	DQ56
21	DQ10	51	V _{DDQ}	81	DQ33	111	DQ57
22	DQ11	52	CKE0	82	V _{SS}	112	V _{SS}
23	V _{SS}	53	V _{DD}	83	DQS4#	113	DQS7#
24	DQ16	54	NC	84	DQS4	114	DQS7
25	DQ17	55	NC	85	V _{SS}	115	V _{SS}
26	DQ17	56	V _{DDQ}	86	DQ34	116	DQ58
27	DQS2#	57	A11	87	DQ35	117	DQ59
28	DQS2	58	A7	88	V _{SS}	118	V _{SS}
29	V _{SS}	59	V _{DD}	89	DQ40	119	SDA
30	DQ18	60	A5	90	DQ41	120	SCL

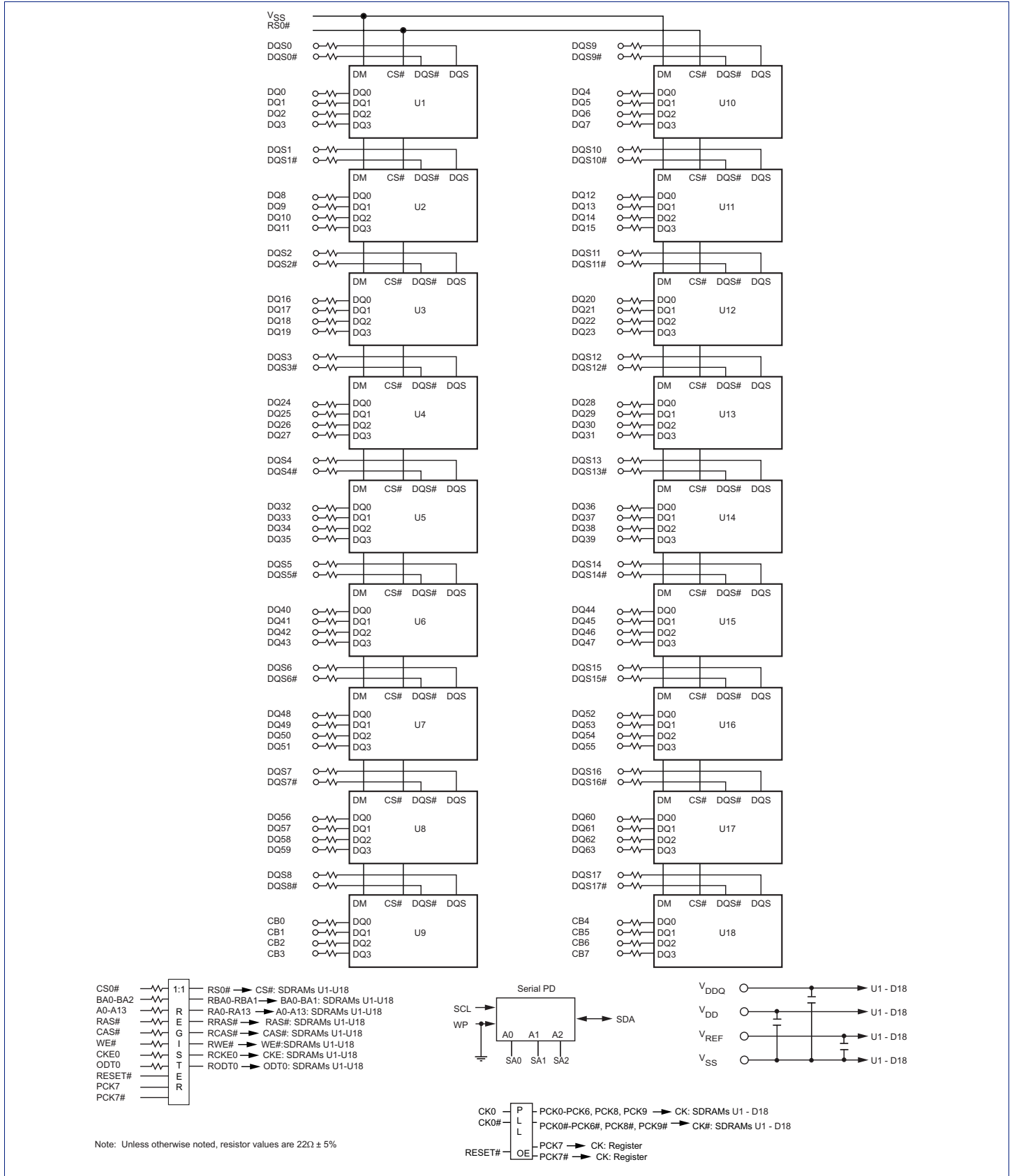
PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL
121	V _{SS}	151	V _{SS}	181	V _{DDQ}	211	DQS14
122	DQ4	152	DQ28	182	A3	212	DQS14#
123	DQ5	153	DQ29	183	A1	213	V _{SS}
124	V _{SS}	154	V _{SS}	184	V _{DD}	214	DQ46
125	DQS9	155	DQS12	185	CK0	215	DQ47
126	DQS9#	156	DQS12#	186	CK0#	216	V _{SS}
127	V _{SS}	157	V _{SS}	187	V _{DD}	217	DQ52
128	DQ6	158	DQ30	188	A0	218	DQ53
129	DQ7	159	DQ31	189	V _{DD}	219	V _{SS}
130	V _{SS}	160	V _{SS}	190	BA1	220	NC
131	DQ12	161	CB4	191	V _{DDQ}	221	NC
132	DQ13	162	CB5	192	RAS#	222	V _{SS}
133	V _{SS}	163	V _{SS}	193	S0#	223	DQS15
134	DQS10	164	DQS17	194	V _{DDQ}	224	DQS15#
135	DQS10#	165	DQS17#	195	ODT0	225	V _{SS}
136	V _{SS}	166	V _{SS}	196	A13 (NC)	226	DQ54
137	NC	167	CB6	197	V _{DD}	227	DQ55
138	NC	168	CB7	198	V _{SS}	228	V _{SS}
139	V _{SS}	169	V _{SS}	199	DQ36	229	DQ60
140	DQ14	170	V _{DDQ}	200	DQ37	230	DQ61
141	DQ15	171	NC, CKE1	201	V _{SS}	231	V _{SS}
142	V _{SS}	172	V _{DD}	202	DQS13	232	DQS16
143	DQ20	173	NC	203	DQS13#	233	DQS16#
144	DQ21	174	NC	204	V _{SS}	234	V _{SS}
145	V _{SS}	175	V _{DDQ}	205	DQ38	235	DQ62
146	DQS11	176	A12	206	DQ39	236	DQ63
147	DQS11#	177	A9	207	V _{SS}	237	V _{SS}
148	V _{SS}	178	V _{DD}	208	DQ44	238	V _{DDSPD}
149	DQ22	179	A8	209	DQ45	239	SA0
150	DQ23	180	A6	210	V _{SS}	240	SA1

Pin Configurations Descriptions

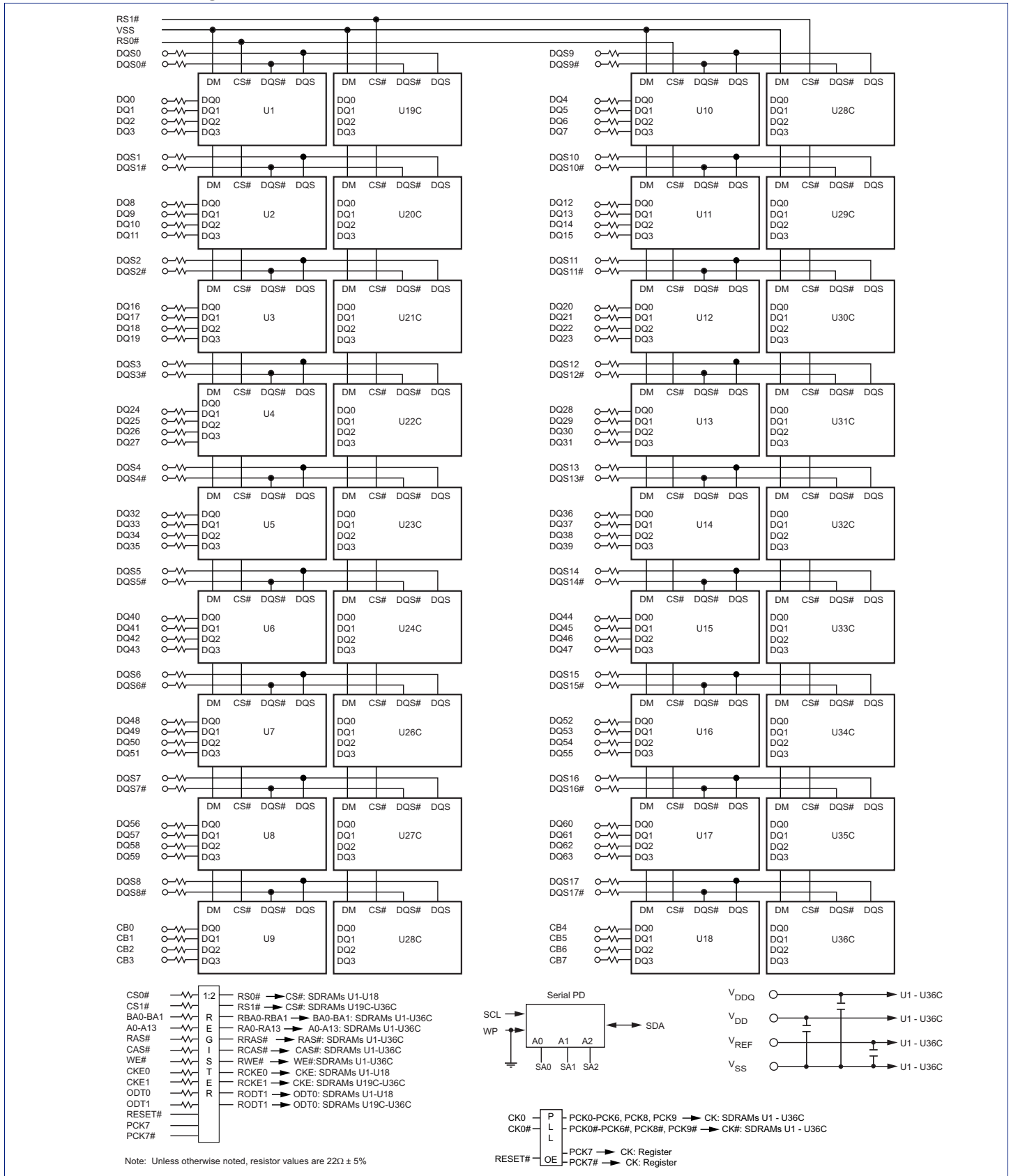
SYMBOL	TYPE	POLARITY	INPUT FUNCTION
CK0, CK0#	Input	Cross Point	The system clock inputs. All address and command lines are sampled at the crossing point of the rising edge of CK and the falling edge of CK. An on-board DLL circuit is driven from the clock inputs and output timing for read operations is synchronized to the input clock.
CKE [1:0]	Input	Active High	CKE high activates and CKE low deactivates internal clock signals and device input buffers and output drivers of the SDRAMs. Taking CKE low provides Precharge Power-Down and Self-Refresh operation (all banks idle), or Active Power-Down (row Active in any bank).
CS# [1:0]	Input	Active	Enables the associated SDRAM command decoder when low and disables decoder when high. When decoder is disabled, new commands are ignored and previous operations continue. The input signals also disable all outputs (except CKE and ODT) of the register(s) on the DIMM when both inputs are high. When both CS[1:0] are high, all register outputs (except CK, ODT and Chip select) remain in the previous state.
ODT [1:0]	Input	Active	On-Die Termination control signals.
RAS#, CAS#, WE#	Input	Active Low	When sampled at the positive edge of the clock, RAS, CAS and WE define the operation to be executed by the SDRAM.
DM [8:0]	Input	Active	Masks write data when high, issued concurrently with input data; connected to ground ^a .
BA [1:0]	Input	-	Selects which internal SDRAM memory bank is activated.
A [13:0]	Input	Active	During Bank Activate command cycle, Address defines the row address. During a Read or Write command cycle, Address defines the column address. In addition to the column address, A10(=AP) is used to invoke Auto-Precharge operation at the end of the burst read or write cycle. If AP is high, Auto Precharge is selected and BA[1:0] defines the bank to be precharged. If AP is low, Auto-Precharge is disabled. During a Precharge command cycle, AP is used in conjunction with BA[1:0] to control which bank(s) to precharge. If AP is high, all banks will be precharged regardless of the state of BA[1:0]. If AP is low, BA[1:0] are used to define which bank to precharge.
DQ [63:0], CB [7:0]	I/O	-	Data and Check Bit Input /Output pins.
DQS [17:0], DQS# [17:0]	I/O	Cross Point	The data strobes, associated with one data nibble, source with data transfer. In Write mode, the data strobe is sourced by the controller and is centered in the data window. In Read mode the data strobe is sources by the DDR2 SDRAM and is sent at the leading edge of the data window. DQS signals are complements, and timing is relative to the crosspoint of respective DQS and DQS. If the module is to be operated in single ended strobe mode, all DQS signals must be tied on the system board to VSS and DDR2 SDRAM mode registers programmed appropriately.
SA [2:0]	Input	-	These signals are tied at the system planar to either VSS or VDDSPD to configure the serial SPD EEPROM address range.
SDA	I/O	-	This bidirectional pin is used to transfer data into and out of the SPD EEPROM. A resistor maybe connected from the SDA bus line to VDDSPD on the system planar to act as a pullup.
SCL	Input	-	This signal is used to clock data into the SPD EEPROM. A resistor maybe connected from the SCL bus line to VDDSPD on the system planar to act as a pull-up.
RESET#	Input	-	The RESET pin is connected to the RST pin on the register and to the OE pin on the PLL. When low, all register outputs will be driven low and the PLL clocks to the DRAMs and the register(s) will be set to low level. The PLL will remain synchronized with the input clock.
V _{DD} , V _{SS}	Supply	-	Power and ground for the DDR SDRAM input buffers and core logic.
V _{REF}	Supply	-	Reference voltage for the SSTL-18 inputs.
V _{DDSPD}	Supply	-	Serial EEPROM positive power supply, wired to a separated power pin at the connector which supports from 1.7 Volt to 3.6 Volt.

a. Tied to ground in this configuration

Functional Block Diagram: Single Rank

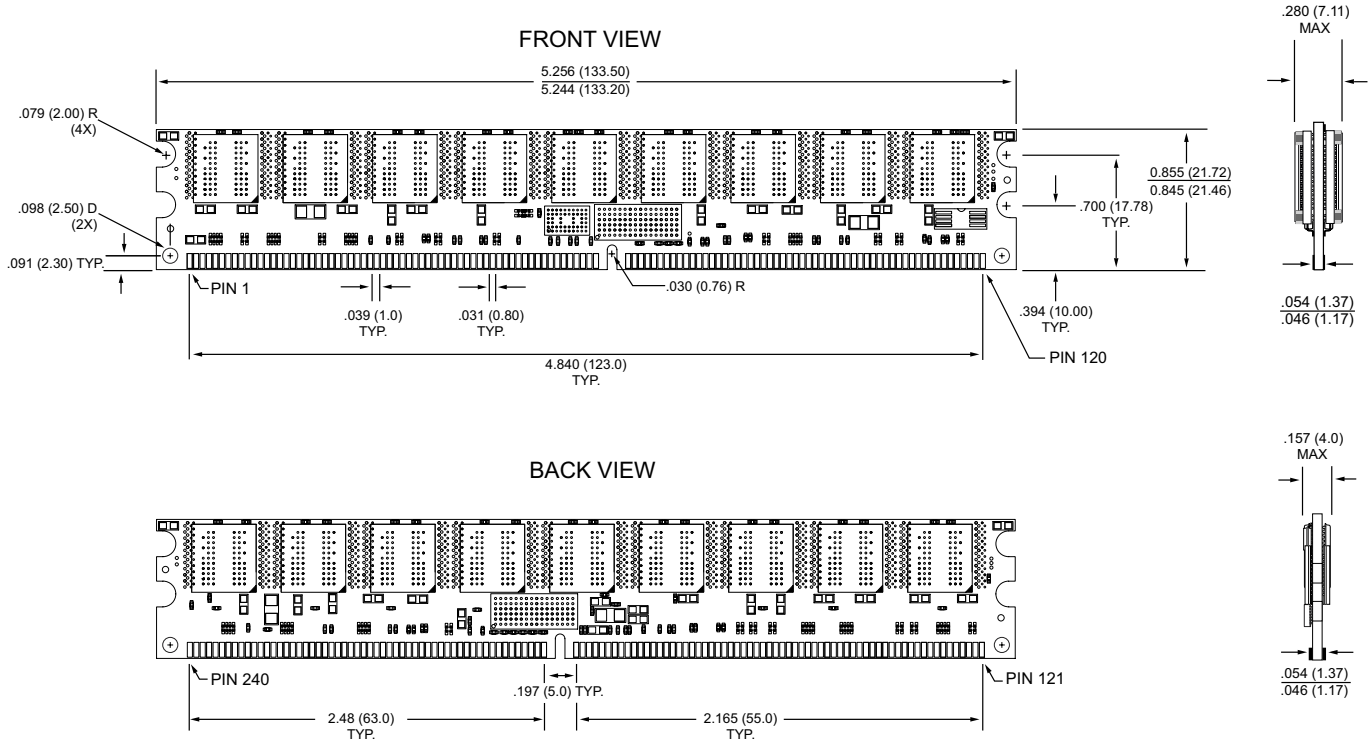


Functional Block Diagram: Dual Rank



Module Dimensions

Units: Inches (Millimeters)



All dimensions in inches (millimeters) $\frac{MAX}{MIN}$ or typical where noted.
Tolerances: ± 0.005 (.13) unless otherwise specified.
This device utilizes 64Mx4 or 128Mx4 DDR2 FBGA SDRAM components.