

## 64Mx72, 128Mx72 PointSeven™ Registered ECC DDR SDRAM DIMM

Registered ECC DDR SDRAM DIMM based on 64Mx4 and 128Mx4, 4-bank, 2.5V FBGA DDR SDRAMs with SPD

### General Description

These small form factor 512MB and 1GB devices are JEDEC standard Double Data Rate DIMMs organized as 64Mx72 and 128Mx72 high density DDR synchronous memory modules. They consist of eighteen CMOS 64Mx4 or 128Mx4, 4-bank, Double Data Rate SDRAMs in 60-ball FBGA packages on a 184-pin glass epoxy substrate. Decoupling capacitors are mounted on the circuit board and in parallel for each SDRAM. The 512MB and 1GB devices are Dual In-line Memory Modules and are intended for mounting in 184-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on the rise and fall of every clock cycle. Range of operating frequencies, programmable latencies allows the same device to be useful for a variety of high bandwidth, high performance memory system applications.

### Features

- $V_{DDSPD} = 2.3V$  to  $+3.6V$
- ECC, 1-bit error detection and correction
- Registered inputs with one-clock delay
- Phase-lock loop (PLL) clock driver to reduce clock loading
- 2.5V I/O (SSTL\_2 compatible)
- Commands entered on each positive CK edge
- Bidirectional data strobe (DQS) transmitted/received with data, i.e., source-synchronous data capture
- Internal pipelined double data rate (DDR) architecture; two data accesses per clock cycle
- Auto Refresh and Self Refresh Modes
- Differential clock inputs (CK and CK#)
- Selectable burst lengths: 2, 4, or 8
- PCB: height 0.7 inch (17.78 mm) 6 layer PCB

#### Ordering Information:

x = DRAM Supplier  
B = Samsung  
L = Legacy  
M = Micron  
S = Infineon

y = Timing  
J = PC2100 CL2  
L = PC2100 CL2.5  
N = PC2700 CL2.5  
P = PC2700 CL2.5  
R = PC3200 CL3.0\*  
U = PC3200 CL3.0\*

### Pin Configurations (Front Side/Back Side)

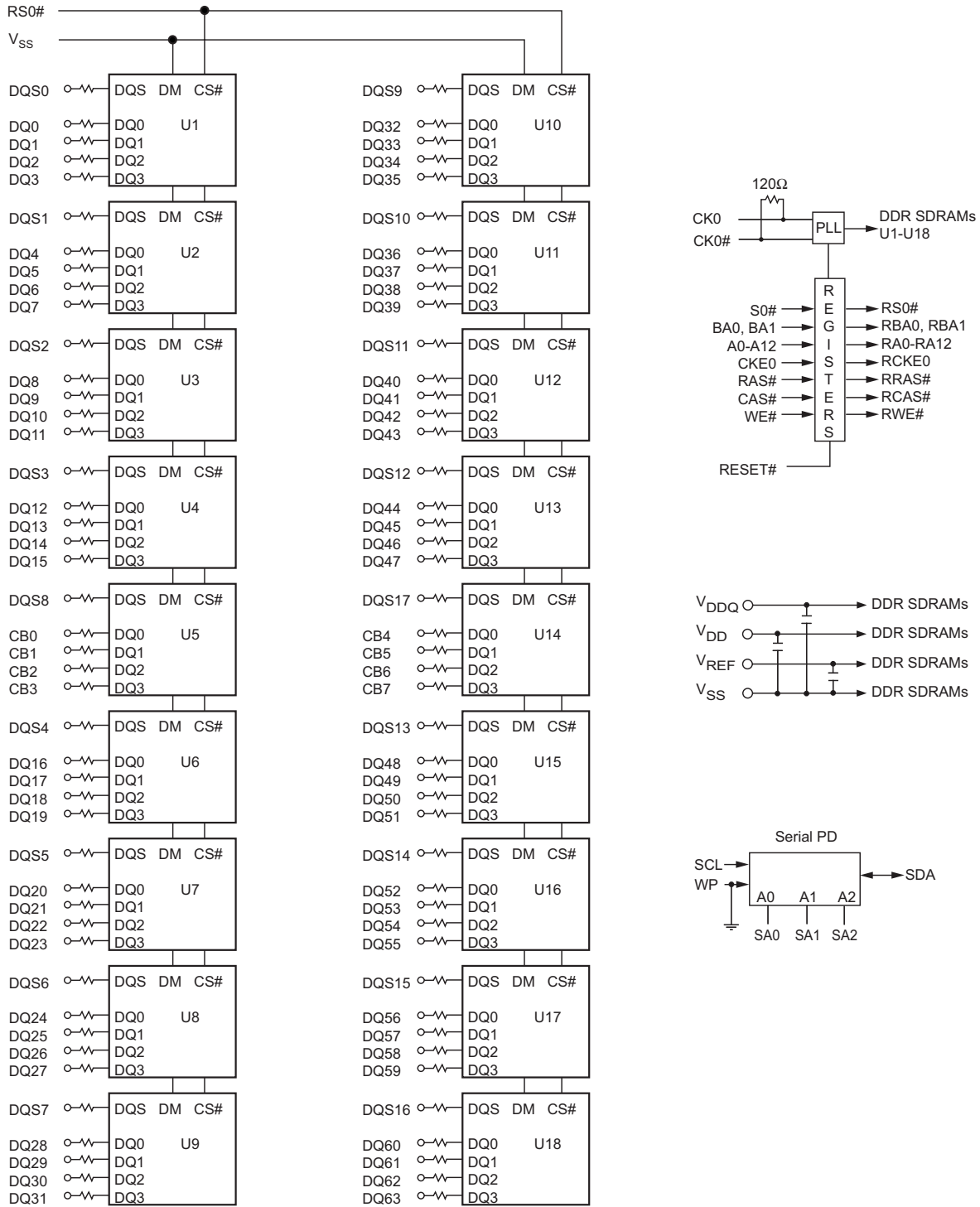
\*2.6V required

PIN	FRONT	PIN	FRONT	PIN	FRONT	PIN	FRONT	PIN	BACK	PIN	BACK	PIN	BACK	PIN	BACK
1	$V_{REF}$	24	DQ17	47	DQS8	70	$V_{DD}$	93	$V_{SS}$	116	$V_{SS}$	139	$V_{SS}$	162	DQ47
2	DQ0	25	DQS2	48	A0	71	NC	94	DQ4	117	DQ21	140	DQS17	163	NC
3	$V_{SS}$	26	$V_{SS}$	49	CB2	72	DQ48	95	DQ5	118	A11	141	A10	164	$V_{DDQ}$
4	DQ1	27	A9	50	$V_{SS}$	73	DQ49	96	$V_{DD}$	119	DQS11	142	CB6	165	DQ52
5	DQS0	28	DQ18	51	CB3	74	$V_{SS}$	97	DQS9	120	$V_{DD}$	143	$V_{DDQ}$	166	DQ53
6	DQ2	29	A7	52	BA1	75	DU	98	DQ6	121	DQ22	144	CB7	167	NC
7	$V_{DD}$	30	$V_{DDQ}$	53	DQ32	76	DU	99	DQ7	122	A8	145	$V_{SS}$	168	$V_{DD}$
8	DQ3	31	DQ19	54	$V_{DDQ}$	77	$V_{DDQ}$	100	$V_{SS}$	123	DQ23	146	DQ36	169	DQS15
9	NC	32	A5	55	DQ33	78	DQS6	101	NC	124	$V_{SS}$	147	DQ37	170	DQ54
10	RESET#	33	DQ24	56	DQS4	79	DQ50	102	NC	125	A6	148	$V_{DD}$	171	DQ55
11	$V_{SS}$	34	$V_{SS}$	57	DQ34	80	DQ51	103	NC	126	DQ28	149	DQS13	172	$V_{DDQ}$
12	DQ8	35	DQ25	58	$V_{SS}$	81	$V_{SS}$	104	$V_{DD}$	127	DQ29	150	DQ38	173	NC
13	DQ9	36	DQS3	59	BA0	82	NC	105	DQ12	128	$V_{DDQ}$	151	DQ39	174	DQ60
14	DQS1	37	A4	60	DQ35	83	DQ56	106	DQ13	129	DQS12	152	$V_{SS}$	175	DQ61
15	$V_{DDQ}$	38	$V_{DD}$	61	DQ40	84	DQ57	107	DQS10	130	A3	153	DQ44	176	$V_{SS}$
16	DU	39	DQ26	62	$V_{DDQ}$	85	$V_{DD}$	108	$V_{DD}$	131	DQ30	154	RAS#	177	DQS16
17	DU	40	DQ27	63	WE#	86	DQS7	109	DQ14	132	$V_{SS}$	155	DQ45	178	DQ62
18	$V_{SS}$	41	A2	64	DQ41	87	DQ58	110	DQ15	133	DQ31	156	$V_{DDQ}$	179	DQ63
19	DQ10	42	$V_{SS}$	65	CAS#	88	DQ59	111	NC	134	CB4	157	S0#	180	$V_{DDQ}$
20	DQ11	43	A1	66	$V_{SS}$	89	$V_{SS}$	112	$V_{DD}$	135	CB5	158	NC	181	SA0
21	CKE0	44	CB0	67	DQS5	90	DU	113	NC	136	$V_{DDQ}$	159	DQS14	182	SA1
22	$V_{DDQ}$	45	CB1	68	DQ42	91	SDA	114	DQ20	137	CK0	160	$V_{SS}$	183	SA2
23	DQ16	46	$V_{DD}$	69	DQ43	92	SCL	115	A12	138	CK0#	161	DQ46	184	$V_{DDSPD}$

## Pin Configurations Descriptions

SYMBOL	TYPE	FUNCTION
CK0 ~ CK0#	Input	Clock: CK, CK# are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK, and negative edge of CK#. Output data (DQs and DQS) is referenced to the crossings of CK and CK#.
CKE0	Input	Clock Enable: CKE HIGH activates and CKE LOW deactivates the internal clock, input buffers, and output drivers. Taking CKE LOW provides PRECHARGE POWER-DOWN and SELF REFRESH operations (all device banks idle), or ACTIVE POWER-DOWN (row ACTIVE in any device bank). CKE is synchronous for POWER-DOWN entry and exit, and for SELF REFRESH entry. CKE is asynchronous for SELF REFRESH exit and for disabling the outputs. CKE must be maintained HIGH throughout read and write accesses. Input buffers (excluding CK, CK#, and CKE) are disabled during POWER-DOWN. Input buffers (Excluding CKE) are disabled during SELF REFRESH. CKE is an SSTL_2 input, but will detect an LCMOS LOW level after VDD is applied.
S0#	Input	Chip Select: S# enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when S# is registered HIGH. S# is considered part of the command code.
RAS#, CAS#, WE#	Input	Command Inputs: RAS#, CAS#, and WE# define the command being entered.
BA0, BA1	Input	Bank Address: BA0 and BA1 define to which device bank an ACTIVE, READ, WRITE, or PRECHARGE command is applied.
A0 ~ A9 A11 ~ A12 A10/AP	Input	Address Inputs: A0-A12 provide the row address for ACTIVE commands, and the column address and auto precharge bit (A10) for READ/WRITE commands, to select one location out of the memory array in the respective device bank. A10 sampled during a PRECHARGE command determines whether the PRECHARGE applies to one device bank (A10 LOW, device bank selected by BA0, BA1) or all device banks (A10 HIGH). The address inputs also provide the op-code during a MODE REGISTER SET command. BA0 and BA1 define which mode register (mode register or extended mode register) is loaded during the LOAD MODE REGISTER command.
RESET#	Input	Asynchronously forces all register outputs LOW when RESET# is LOW. This signal can be used during power-up to ensure CKE is LOW and SDRAM DQs are High-Z.
DQ0 ~ DQ63	Input/ Output	Data I/Os: Data bus.
CB0 ~ CB7	Input/ Output	Data I/Os: Check bits. ECC 1-bit error detection and correction.
DQS0 ~ DQS17	Input/ Output	Data Strobe: Output with READ data, input with WRITE data. DQS is edge-aligned with READ data and is centered in WRITE data. Used to capture data.
V <sub>DD</sub>	Supply	Power supply: +2.5V ±0.2V.
V <sub>DDQ</sub>	Supply	DQ Power supply: +2.5V ±0.2V.
V <sub>SS</sub>	Supply	Ground.
V <sub>DDSPD</sub>	Supply	Serial EEPROM positive power supply, 2.3V to 3.6V.
SDA	Input/ Output	Serial Presence-Detect Data: SDA is a bidirectional pin used to transfer addresses and data into and out of the presence-detect portion of the module.
SCL	Input	Serial Clock for Presence-Detect: SCL is used to synchronize the presence-detect data transfer to and from the module.
SA0 ~ SA2	Input	Presence-Detect Address Inputs: These pins are used to configure the presence-detect device.
DU	-	Do not Use: These pins are not connected on this module but are assigned pins on other modules in this product family.
NC	-	No Connect: These pins should be left uncovered.

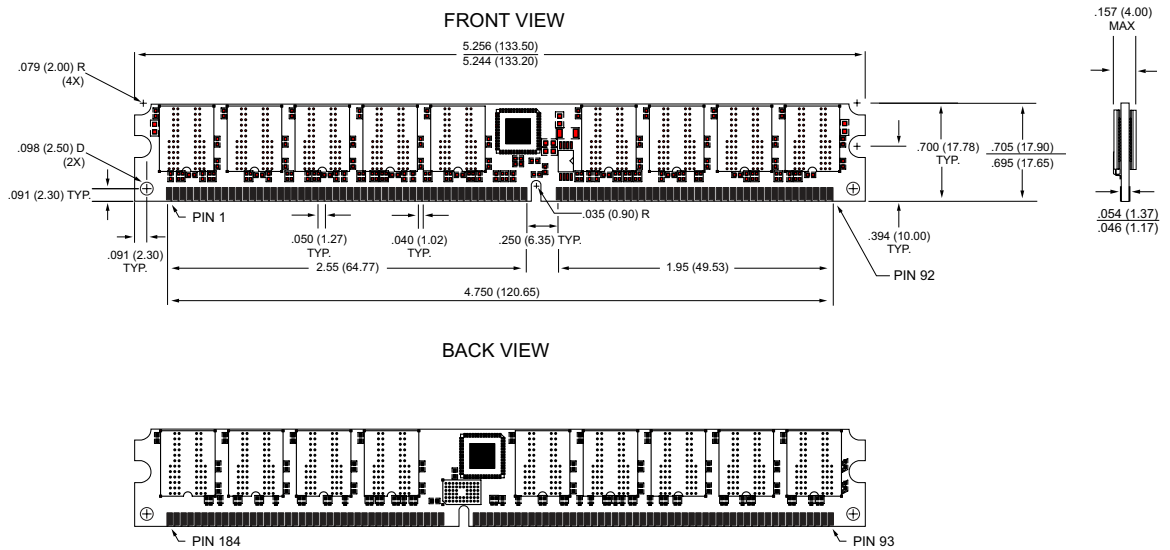
**Functional Block Diagram (Single Rank)**



Note: Unless otherwise noted, resistor values are  $22\Omega \pm 5\%$   
 U1 - U18 = 64Mx4 DDR SDRAMs (256Mbit)  
 U1 - U18 = 128MX4 DDR SDRAMs (512Mbit)

**Module Dimensions**

Units: Inches (Millimeters)



Note: All dimensions in inches (millimeters)  $\frac{MAX}{MIN}$  or typical where noted.